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Chanssa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Cheolsoo PARK**, a citizen of the Republic of Korea, residing at 891-10 Daechi-dong, Gahgnam-gu, Seoul, Korea have invented new and useful **SEMICONDUCTOR TRANSISTORS AND METHODS OF FABRICATING THE SAME**, of which the following is a specification.

SEMICONDUCTOR TRANSISTORS AND METHODS OF FABRICATING THE SAME

TECHNICAL FIELD

[0001] The present disclosure relates to a transistors and, more particularly, to semiconductor transistors and methods of fabricating the same.

BACKGROUND

[0002] As semiconductor devices have become highly integrated, approaches have been developed for decreasing a size of a unit element by reducing a length of a gate electrode, a thickness of a gate insulation layer, and a width of an isolation layer. However, among scaling factors in a semiconductor device, controlling the length of the gate electrode is difficult and, therefore, is expensive to perform. In addition, a short channel effect is known as a characteristic that is difficult to be controlled in a transistor manufacturing process.

[0003] To resolve such problems, U.S. Patent 6,583,017 and U.S. Patent 5,571,738 disclose a method for forming a lightly doped drain (hereinafter referred to as "LDD") region by an ion implantation process.

[0004] However, an improved process is still required that is capable of easily controlling the length of the gate electrode and suppressing the short channel effect.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figs. 1 and 4 illustrate cross sectional views sequentially showing an example disclosed process of fabricating a transistor.

DETAILED DESCRIPTION

[0006] Referring to Fig. 1, after cleaning a semiconductor substrate 1 in which an active region is isolated from an inactive region by isolators 2, an oxide layer, which acts as a buffer insulation layer 3, is thermally grown and a nitride layer as a first insulation layer 4 is thickly deposited thereon.

[0007] A first photoresist pattern (not shown) for forming a gate region is formed on the first insulation layer 4 by a photolithography process. The first insulation layer 4 and the buffer insulation layer 3 may be sequentially etched by an anisotropic dry etching process using the first photoresist pattern as a mask. In the anisotropic dry etching process, the buffer insulation layer 3 is not entirely removed and remains with a small thickness. The first photoresist pattern is then removed. A polysilicon is deposited on sidewalls of the first insulation layer 4 and the buffer insulation layer 3 by using an in-situ doping process, thereby forming poly electrodes 5 for an LDD. As a result, the poly electrodes 5 are formed on an active region of a semiconductor

substrate and separated in two parts facing each other, which defines a length of a gate electrode to be formed later.

[0008] Subsequently, a local channel region 6 is formed into the semiconductor substrate by performing a local ion implantation process under the buffer insulation layer, i.e., under the gate electrode 8 to be formed later. The local channel region 6 serves to prevent lateral diffusions of a source electrode 10a and a drain electrode 10b to be formed later, thereby suppressing the short channel effect.

[0009] As shown in Fig. 2, after the buffer oxide layer 3 having a thickness of some tens of angstroms (Å) remaining in the gate region is removed by cleaning, a gate insulation layer 7 is deposited on the sidewalls of the poly electrode 5 and the exposed portion of the semiconductor substrate. A gate electrode material is deposited on the gate insulation layer 7 and a blanket etchback process or a chemical mechanical polishing (CMP) process is performed thereon, thereby forming the gate electrode 8. In other words, the gate insulation layer 7 is formed with a trench-shape on the sidewalls of the poly electrodes 5 and on the semiconductor substrate above the local channel region 6 and the gate electrode material is filled into the trench-shaped region formed by the gate insulation layer 7.

[0010] Referring to Fig. 3, the first insulation layer 4 and an upper part of the buffer insulation layer 3 are removed by performing the blanket etchback process. A silicide 9 is formed on the outside surfaces of the gate electrode 8 and the poly electrode 5 by performing a salicidation process. Subsequently, the source electrode 10a and the drain electrode 10b are formed by implantating high density impurity ions into the semiconductor substrate on the left and the right side of the gate electrode 8. A nitride layer having a thickness of some hundreds of Å as a second insulation layer 11 then is deposited on the resultant structure.

[0011] In case TiN/W is deposited as the gate electrode material, the silicide forming process may be omitted. Further, although according to one example the source electrode 10a and the drain electrode 10b are formed by the ion implantation process, in other examples they may be formed by a selective epitaxial silicon growth process or an in-situ doping process of polysilicon. Also, the source electrode 10a and the drain electrode 10b may be formed by annealing after deposition of boro-silicate glass (BSG) or phospho-silicate glass (PSG).

[0012] As shown in Fig. 4, a third insulation layer 12 is thickly deposited on the resultant structure and a second photoresist pattern (not shown) for forming a gate plug 13a, a source contact plug 13b and a drain contact plug 13c is formed thereon.

Subsequently, contact holes through which the gate electrode 8, the source electrode 10a and the drain electrode 10b are exposed are formed by etching the third insulation layer 12, the second insulation layer 11 and the buffer insulation layer 3 using the second photoresist pattern as a mask. The second photoresist pattern is then removed. After depositing a conductive material on the entire surface of the resultant structure to fill the contact holes, the gate plug 13a, the source contact plug 13b, and the drain contact plug 13c are formed by planarizing the surface of the resultant structure using a CMP process or an entire etching process.

[0013] In accordance with the example processes disclosed herein, a transistor has poly electrodes for an LDD without performing an LDD ion implantation process, thereby controlling a length of a gate electrode at a low cost. Also, a local channel ion implantation process may be performed on the semiconductor substrate under the gate electrode, thereby easily suppressing a short channel effect.

[0014] As disclosed herein, one example method of fabricating a transistor may include sequentially depositing a buffer insulation layer and a first insulation layer on a semiconductor substrate, etching the first insulation layer and the buffer insulation layer and forming poly electrodes for a lightly doped drain (LDD) on sidewalls of the etched portion thereof, forming a local channel region into the semiconductor

substrate under the poly electrodes by performing an local channel ion implantation process, and forming a gate insulation layer on surfaces of the poly electrodes and the semiconductor substrate above the local channel region. The example method may also include forming a gate electrode by depositing a gate electrode material on the gate insulation layer and forming a source and drain region.

[0015] Additionally, as disclosed herein, an example transistor may include poly electrodes for a lightly doped drain (LDD) formed on sidewalls of a gate region, a local channel region formed into a semiconductor substrate under the poly electrodes, a gate insulation layer formed with a trench-shape on sidewalls of the poly electrodes and on the semiconductor substrate above the local channel region, and a gate electrode filled into the trench-shaped region formed by the gate insulation layer. The example transistor may also include a source electrode and a drain electrode formed into the semiconductor substrate on the opposite sides of the gate electrode and a gate plug.

[0016] Although certain example methods are disclosed herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers every apparatus, method and article of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.